CLAIMS

What is claimed is:

1.   A system comprising:

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a processor;

a main memory operably coupled to the processor;

10   a cache memory operably coupled to the processor; and

a host controller coupled between the processor and the main memory, the host controller

comprising:

a memory controller operably coupled to the main memory;

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a processor controller operably coupled to the processor;

a coherency controller operably coupled to the cache memory; and

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an internal bus structure configured to couple each of the memory controller , the

processor controller and the coherency controller to each other, the internal

bus structure comprising a plurality of individual buses, wherein each of the

individual buses comprises a unidirectional bus configured to transmit only one signal type.

5   2.   The system, as set forth in claim 1, wherein each of the plurality of individual buses is coupled only between two of the memory controller, the processor controller and the coherency controller.

10   3.   The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the memory controller and the processor controller.

       4.   The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the memory controller and the coherency controller.

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       5.   The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the processor controller and the coherency controller.

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6.   The system, as set forth in claim 1, wherein each of the plurality of individual buses is configured to transmit only one respective signal type and wherein each respective signal type corresponds to a single transaction in a request operation.

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7.   The system, as set forth in claim 6, wherein each respective signal type includes an identification tag.

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8.   The system, as set forth in claim 7, wherein the identification tag comprises a source identification, a destination identification, and a cycle identification.

9.   The system, a set forth in claim 8, wherein the cycle identification comprises a

15   toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete.

10.   The system, as set forth in claim 1, wherein the processor comprises the cache

20   memory.

11. The system, as set forth in claim 1, comprising:

a plurality of processor buses;

5   a plurality of processing units, wherein each processing unit is coupled to a respective

one of the plurality of processor buses; and

a plurality of processor controllers, each processor controller corresponding to a

respective one of the plurality of processor buses, wherein the processor

10   controllers are not directly coupled to each other via the internal bus structure.

12. An internal bus structure comprising a plurality of individual buses, each of the

individual buses comprising a unidirectional bus configured to transmit only one signal type.

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13. The internal bus structure, as set forth in claim 12, wherein each individual bus is

coupled between only a first controller and a second controller.

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14. The internal bus structure, as set forth in claim 13, wherein the first controller

comprises a processor controller .

15.   The internal bus structure, as set forth in claim 13, wherein the second controller comprises one of a memory controller and a coherency controller .

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16.   The internal bus structure, as set forth in claim 12, wherein each of the individual buses is configured to transmit only one signal type and wherein each signal type corresponds to a single transaction in a request operation.

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17.   The internal bus structure, as set forth in claim 16, wherein each signal type includes an identification tag.

18.   The internal bus structure, as set forth in claim 17, wherein the identification tag

15   comprises a source identification, a destination identification and a cycle identification.

19.   The internal bus structure, as set forth in claim 18, wherein the cycle identification includes a toggle bit configured to free the cycle identification for re-use before each transaction

20   in the request operation is complete.